IN THE CLAIMS

1. (Currently Amended) A circuit comprising:

at least one first power amplifier;

at least one first matching circuit coupled to the at least one first power amplifier; and,

at least one first filter coupled to the at least one first matching circuit,

at least one second power amplifier;

at least one second matching circuit coupled to the at least one second power amplifier; and,

at least one second filter coupled to the at least one second matching circuit;

wherein a signal received by the at least one first power amplifier is transmitted to the at least one first filter through the at least one first matching circuit and a signal received by the at least one second power amplifier is transmitted to the at least one second filter through the at least one second matching circuit;

at least one switch coupled to the at least one first and at least one second filters; and

a decoder coupled to provide control signals to the at least one first and at least one second power amplifiers and to said at least one switch.

2. (Cancelled).

3. (Cancelled).

4. (Cancelled)

5. (Cancelled)

6. (Cancelled).

7. (Original) The circuit of claim 1, wherein the at least one first power amplifier, the at least one first matching network, and the at least one first filter are all disposed on a leadframe.

8. (Currently Amended) ~~The circuit of claim 7,~~ A circuit comprising:

at least one first power amplifier;

at least one first matching circuit coupled to the at least one first power amplifier; and,

at least one first filter coupled to the at least one first matching circuit,

at least one second power amplifier;

at least one second matching circuit coupled to the at least one second power amplifier; and,

at least one second filter coupled to the at least one second matching circuit;

wherein a signal received by the at least one first power amplifier is transmitted to the at least one first filter through the at least one first matching circuit and a signal received by the at least one second power amplifier is transmitted to the at least one second filter through the at least one second matching circuit; and

a decoder coupled to provide control signals to the at least one first and at least one second power amplifiers;

wherein the at least one first power amplifier, the at least one first matching network, and the at least one first filter are all disposed on a leadframe, said ~~wherein~~ the leadframe ~~includes~~ including forty-two connector pads.

9. (Currently Amended) ~~The circuit of claim 1,~~ A circuit comprising:

at least one first power amplifier;

at least one first matching circuit coupled to the at least one first power amplifier; and,

at least one first filter coupled to the at least one first matching circuit,

at least one second power amplifier;

at least one second matching circuit coupled to the at least one second power amplifier; and,

at least one second filter coupled to the at least one second matching circuit;

wherein a signal received by the at least one first power amplifier is transmitted to the at least one first filter through the at least one first matching circuit and a signal received by the at least one second power amplifier is transmitted to the at least one second filter through the at least one second matching circuit;

at least one switch coupled to the at least one first and at least one second filters; and

a decoder coupled to provide control signals to the at least one first and at least one second power amplifiers; wherein the at least one switch comprises a single pole six throw switch.

10. (Previously Presented) The circuit of claim 1, wherein the at least one switch is coupled to at least one antenna terminal.

11. (Previously Presented) The circuit of claim 1, wherein the at least one switch is coupled to at least one reception terminal.

12. (Cancelled).

13. (Cancelled).

14. (Original) The circuit of claim 1, wherein the at least one first filter comprises

a low pass filter.

15. (Previously Presented) The circuit of claim 1, wherein the at least one first and at least one second filters both comprise low pass filters.

16. (Previously Presented) The circuit of claim 1, wherein the at least one first and second power amplifiers, the at least one first and second matching networks, and the at least one first and second filters are all disposed on a leadframe.

17. (Cancelled).

18. (Cancelled)

19. (Currently Amended) A telecommunications system comprising:

an antenna; and,

a front end module coupled to the antenna,

wherein the front end module includes at least one first power amplifier, at least one first matching circuit coupled to the at least one first power amplifier, and at least one first filter coupled to the at least one first matching circuit, wherein a signal received by the at least one first power amplifier is transmitted to the at least one first filter through the at least one first matching circuit.;

at least one second power amplifier;

at least one second matching circuit coupled to the at least one second power amplifier;

at least one second filter coupled to the at least one second matching circuit, wherein a signal received by the at least one second power amplifier is transmitted to the at least one second filter through the at least one second matching circuit;

at least one switch coupled to the at least one first and at least one second filters; and

a decoder coupled to provide control signals to the at least one first and at least one second power amplifiers and to said at least one switch.

20. (New) The circuit of claim 1 wherein said circuit is embodied on a single Fine Pitch Quad No-Lead Package.

21. (New) The circuit of claim 1 wherein said first and second amplifiers are dual band amplifiers.

22. (New) The circuit of claim 21 wherein said first and second amplifiers are Indium-Gallium Phosphide Hetero-Bipolar Transistor power amplifiers.

23. (New) The circuit of claim 22 wherein said decoder is a Complementary Metal Oxide Semiconductor controller.

24. (New) The circuit of claim 1 wherein said switch is a Pseudo Morphic High Electron Mobility Transistor switch.

25. (New) The circuit of claim 1 wherein said switch selectively switches between an output of said first filter, an output of said second filter, a first receive port, and second receive port, a third receive port, and a fourth receive port, under control of said decoder.

26. (New) The circuit of claim 9 wherein said single pole six throw switch is coupled to select between an output of said first filter, an output of said second filter, a first receive port, and second receive port, a third receive port, and a fourth receive port.

27. (New) The circuit of claim 19 wherein said front end module is embodied on a single Fine Pitch Quad No-Lead Package.

28. (New) The circuit of claim 27 wherein said telecommunications system is a cellular telephone handset.

29. (New) The circuit of claim 19 wherein said switch selectively couples one of an output of said first filter, an output of said second filter, a first receive port, and second receive port, a third receive port, and a fourth receive port to said antenna, under control of said decoder.